REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in the present application. Claims 1 and 2 are amended by the present amendment.

Claim amendments find support in the claims as originally filed and in the specification at least at page 9, line 33 to page 10, line 4. Thus, no new matter is added.

This amendment is submitted in accordance with 37 C.F.R. § 1.116, which after final rejection permits entering of amendments, canceling claims, complying with any requirement of form expressly set forth in a previous Office Action, or presenting rejected claims in better form for consideration on appeal. It is therefore respectfully requested that the present amendment be entered under 37 C.F.R. § 1.116.

In the outstanding Office Action, Claims 1-4 and 10-12 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,523,136 to Higashida in view of U.S. Patent No. 6,687,857 to Iwata et al. (herein "Iwata"); and Claims 5-9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Higashida in view of Iwata and U.S. Patent No. 5,566,303 to Tashiro et al. (herein "Tashiro").

Initially, Applicant respectfully notes that the references in the Information Disclosure Statement filed October 28, 2004 were not indicated as having been considered by the Examiner. Accordingly, Applicant requests that a signed PTO Form-1449 be provided indicating consideration of those references.

Further, Applicant respectfully traverses the rejections of Claims 1-12 under 35 U.S.C. § 103(a) as unpatentable over Higashida in view of Iwata and Tashiro.

Amended Claim 1 is directed to a system LSI formed on one chip including a storage circuit storing an operation program and a debug backup functional program, processor

circuit with a program counter, and a peripheral circuit including a function block. In addition, the system LSI includes a selection means for optionally selecting one output of the program counter, the computing unit and the register in the processor circuit, at least one output of the storage circuit, and one output of a plurality of internal signals in the peripheral circuit including an output of the functional block. Further, the system LSI also includes a selection control means for controlling selection of a result signal from any operation process in any place of the processor circuit, the storage circuit and the peripheral circuit, based on a selection signal that is supplied from the outside of the system LSI via an external terminal. The system LSI also includes a debug backup circuit for carrying out a debug to a bug caused by any operation process, on the basis of the debug backup functional program that is stored in the storage circuit.

Applicant respectfully submits that Higashida does not teach or suggest a system LSI on one chip including a debug backup circuit for carrying out a debug. As noted in the outstanding Office Action, Higashida describes peripheral circuits in FIG. 1.[1] However, Higashida describes only peripheral circuits 20 and 30 in FIG 1. Further, Higashida describes that an internal bus is further connected to peripheral circuits such as a bus arbiter, which are not shown in the figure for simplicity reason.[2] Thus, although Higashida indicates peripheral circuits in an LSI chip from this description, Higashida indicates that internal signals are outputted from the peripheral circuits to an outside of the LSI as an object of the debug. Hence, it appears that Higashida does not have internal peripheral circuits as an object of debugging, and thus does not appear to teach or suggest "[a] system LSI formed on one chip, comprising . . . a peripheral circuit [and] selection means for optionally selecting . . . one output of a plurality of internal signals in said peripheral circuit," as recited in Claim 1.

[1] Office Action at page 3, lines 1-2.
[2] Higashida at column 1, lines 52-55.

Further, Applicant respectfully submits that Higashida does not teach or suggest the claimed selection means, and further Applicant traverses the assertion in the outstanding Office Action that Higashida discloses selection means at column l, lines 22-37, at column 7, lines 15-30, and in FIGS. 2 and 3.[3] The cited column 1 passage does not describe a selection means. The cited column 7 passage of Higashida indicates that an instruction execution processing portion 2c transmits a control signal via a CPU internal bus 2d. However, Applicant submits that Higashida does not disclose the selection means and a selection control means in that cited passage. Further, Higashida, shows a detailed configuration of a CPU core in FIG. 2 and a detailed configuration of a multiplexer 8 in FIG. 3. However, Higashida indicates that the multiplexer 8 selects any of signals from the internal bus corresponding to test mode instruction signal TPl and TP2 that are externally supplied via signal input terminal 9, which is different than the claimed approach in which selection control means 4, internally provided in the LSI, controls the selection means 30.

Further, Applicant respectfully traverses the assertion in the Office Action that Higashida performs "a selector control by way of a signal via an external terminal."[4] Higashida does not disclose a selection control means that outputs the selection control signal to the selection means responsive to the external selection signal. As indicated in FIG. 1, the device of Higashida merely includes a DSU-adapted debug device 20 that is externally provided and controls DSU 2a via pin terminal 10 of the LSI. Furthermore, Higashida indicates that the detailed control for the internal bus is performed by reading the program through the terminal 22 of the DSU-adapted debug device 20 from the internal bus signal display software (SF) 30a provided in the computer 30. On the contrary, a one-chip system LSI according to the present invention comprises a storage circuit including a debug backup program for internally controlling debugging in the LSI. Thus, Higashida does not teach or

[3] Office Action at page 3, lines 3-5.
[4] Office Action at page 3, line 5.

suggest "[a] system LSI being formed on one chip, comprising . . . a storage circuit in which an operation program and a debug backup functional program are stored," as recited in amended Claim 1.

Further, Applicant respectfully submits that Iwata and Tashiro also do not disclose the claimed features. Thus, the combined teachings of Higashida, Iwata and Tashiro do not teach or suggest the features of the independent claims. Accordingly, Applicant respectfully submits that independent Claim 1 and claims depending therefrom are allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 08/03)

EHK:ZSS:dnf
I:\ATTY\ZS\21'S\211\211200US\211200-AM.122904.DOC